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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,247	11/08/2001	Min Kim	SEC.853	5037

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JONES VOLENTINE, P.L.L.C.
Suite 150
12200 Sunrise Valley Drive
Reston, VA 20191

EXAMINER

GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 02/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/986,247

Applicant(s)

KIM ET AL.

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-24, 26 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-24, 26 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. This Office Action is in response to the Amendment filed October 20, 2003 and the Request for continued examination filed November 20, 2003.

Claims 1-10, 25, and 28 are canceled.

Claims 11-24 and 26-27 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 20, 2003 has been entered.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 11-12 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) in view of Chang et al. (U.S. 6,326,310).

Bohr teaches a method of manufacturing a trench isolation structure (Abstract). Bohr shows sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate, patterning the pad oxide layer and the hard mask layer using photolithography, etching a portion of the semiconductor substrate to form a shallow trench, and forming a thermal oxide layer along inner walls of the semiconductor substrate that define the shallow trench (Fig. 1, 3A, col. 4, lines 64-67, col. 5, lines 15-20, and 59-65).

Furthermore, Bohr shows the lateral portions of the thermal oxide having a curvilinear section profile at an interface with the upper surface of the semiconductor substrate and a central portion. Bohr shows etching away the central portion of the thermal oxide layer and the semiconductor substrate to extend the shallow trench deeper into the semiconductor substrate (col. 6, lines 10-15, 40-48).

Bohr teaches forming a buffer layer over the deep trench by thermal oxidation (high temperature oxide layer) (col. 6, lines 40-45), filling the deep trench with a first oxide layer (CVD deposited silicon dioxide or other oxide formation techniques),

Art Unit: 2822

planarizing the structure, and removing the hard mask pattern (Fig. 2, col. 7, lines 20-27, 40-45, 60-62).

Regarding claims 11-12 and 22-24, Bohr fails to show using the hard mask pattern as a mask to extend the shallow trench, forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern and etching a portion of the semiconductor substrate using the hard mask pattern and the spacer as a mask to form the shallow and deep trenches. However, Bohr teaches various techniques and/or various other materials may be used for the masking and etching of the trenches (col. 7, lines 5-9). In addition, Chang et al. shows forming the spacers along sidewalls of the hard mask pattern and the pad oxide pattern and etching a portion of the semiconductor substrate using the hard mask pattern and the spacers as a mask (Fig. 3-5, col. 4, lines 1-9, 22-30, col. 5, lines 10-30, col. 6, lines 4-10).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bohr reference by including the step of forming the spacer and using the spacer and the hard mask pattern as a mask in order to use any desired trench profile (Chang et al., col. 25-30).

5. Claims 17, 19, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) in view of Yoo et al. (U.S. 6,033,969).

Bohr teaches forming a thermal oxide layer on a portion of the upper surface of the semiconductor substrate where a trench isolation layer will be formed and etching away portions of the thermal oxide layer and the semiconductor substrate (Fig. 3B-3C, col. 6, lines 10-12). Bohr teaches forming a buffer layer over the deep trench by thermal

oxidation (high temperature oxide layer) (col. 6, lines 40-45), filling the deep trench with a first oxide layer (CVD deposited silicon dioxide or other oxide formation techniques), planarizing the structure, and removing the hard mask pattern (Fig. 2, col. 7, lines 20-27, 40-45, 60-62).

Regarding claims 17, 19, and 26, Bohr does not specifically show forming a thermal oxide layer on a portion of the flat upper surface of the semiconductor substrate between respective portions of the pad oxide pattern. Bohr does not specifically show the thermal oxide having lateral portions with sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate. However, Bohr teaches the steps may be reordered, modified, or even improved upon and that other processing steps may be used. Bohr discloses various other techniques and/or various other materials may be used for the masking and etching the trenches (col. 6, lines 49-65, col. 7, lines 5-8).

Furthermore, Yoo et al. teaches forming a thermal oxide layer on a portion of the flat upper surface of the semiconductor substrate between respective portions of the pad oxide pattern (Fig. 4-5, col. 2, lines 50-65, col. 3, lines 1-20, 60-65). Yoo et al. discloses the thermal oxide having lateral portions with sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate (Fig. 6, col. 2, lines 30-40, col. 3, lines 65-67). Yoo et al. teaches etching the central portion of the thermal oxide layer and the lateral portions are left (Fig. 6-8, col. 4, lines 4-15, 40-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bohr reference by including the thermal oxide having

Art Unit: 2822

lateral portions with sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate as taught by Yoo et al. in order to provide trenches having protected corners and would avoid dislocations at the corner of the trenches (Yoo et al., col. 2, lines 7-40)

6. Claims 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) in view of Yoo et al. (U.S. 6,033,969) as applied to claims 17, 19, and 26 above, and further in view of Chang et al. (U.S. 6,326,310).

Regarding claims 18 and 27, the combination of Bohr and Yoo et al. does not specifically show forming a spacer along sidewall of the hard mask pattern and the pad oxide pattern and using the spacer as a mask. However, Bohr teaches various techniques and/or various other materials may be used for the masking and etching of the trenches (col. 7, lines 5-9). In addition, Chang et al. shows forming the spacers along sidewalls of the hard mask pattern and the pad oxide pattern and etching a portion of the semiconductor substrate using the hard mask pattern and the spacers as a mask (Fig. 3-5, col. 4, lines 1-9, 22-30, col. 5, lines 10-30, col. 6, lines 4-10).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Bohr and Yoo et al. by including the step of forming the spacer and using the spacer and the hard mask pattern as a mask as taught Chang et al. in order to use any desired trench profile (Chang et al., col. 25-30).

Art Unit: 2822

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) and Yoo et al. (U.S. 6,033,969) as applied to claims 17, 19, and 26 above, and further in view of Benedict et al. (U.S. 5,763,315).

Regarding claim 20, the combination of Bohr and Yoo et al. fails to show forming a second oxide layer between the liner and the first oxide layer. However, Benedict et al. shows the step of forming the second oxide layer between the liner and the first oxide layer (Fig. 2B-2E, col. 3, lines 60-63, col. 4, lines 18-21).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include the step of forming the second oxide layer between the liner and the first oxide layer as taught Benedict et al. in order to reduce trap density (Benedict et al., col. 1, lines 59-63).

8. Claims 13-14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) and Chang et al. (U.S. 6,326,310) as applied to claims 11-12 and 22-24 above, and further in view of Benedict et al. (U.S. 5,763,315).

Regarding claims 13-14, the combination of Bohr and Chang et al. fails to show forming a second oxide layer between the liner and the first oxide layer. However, Benedict et al. shows the step of forming the second oxide layer between the liner and the first oxide layer (Fig. 2B-2E, col. 3, lines 60-63, col. 4, lines 18-21).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include the step of forming the second oxide layer between the liner and the first oxide layer as taught Benedict et al. on the combination of Bohr and Chang et al. in order to reduce trap density (Benedict et al., col. 1, lines 59-63).

Art Unit: 2822

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) and Yoo et al. (U.S. 6,033,969) as applied to claims 17, 19, and 26 above, and further in view of Hashimoto et al. (U.S. 6,027,983).

Regarding claim 21, the combination of Bohr and Yoo et al. fails to show the silicon layer being monocrystalline, the step of terminating the etching of the semiconductor substrate at an interface between two of the respective of the SOI structure. However, Hashimoto et al. shows forming a deep trench on a semiconductor substrate having a SOI structure. Hashimoto et al. shows the SOI structure comprising a monocrystalline silicon layer, terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure (Fig. 7, col. 8, lines 50-55, col. 9, lines 40-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Bohr and Yoo et al. by including the use of the SOI structure as taught by Hashimoto et al. because Bohr suggested that the process could be employed in a variety of applications and in order to improved yield and reliability (Hashimoto et al., col. 2, lines 10-24; Bohr, col. 8, lines 13-20, 32-38).

10. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) and Chang et al. (U.S. 6,326,310) as applied to claims 11-12 and 22-24 above, and further in view of Hashimoto et al. (U.S. 6,027,983).

Regarding claims 15-16, the combination of Bohr and Chang et al. fails to show the silicon layer being monocrystalline, the step of terminating the etching of the

Art Unit: 2822

semiconductor substrate at an interface between two of the respective of the SOI structure. However, Hashimoto et al. shows forming a deep trench on a semiconductor substrate having a SOI structure. Hashimoto et al. shows the SOI structure comprising a monocrystalline silicon layer, terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure (Fig. 7, col. 8, lines 50-55, col. 9, lines 40-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Bohr and Chang et al. by including the use of the SOI structure as taught by Hashimoto et al. because Bohr suggested that the process could be employed in a variety of applications and in order to improved yield and reliability (Hashimoto et al., col. 2, lines 10-24; Bohr, col. 8, lines 13-20, 32-38).

Response to Arguments

11. Applicant's arguments with respect to claims 11-24 and 26-27 have been considered but are moot in view of the new ground(s) of rejection. Claim Rejection USC 112 has been withdrawn.

Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Graitmann et al. (U.S. 6,207,494) shows several steps related to applicant's disclosure.

Art Unit: 2822

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.


Maria Guerrero
Primary Examiner
January 23, 2004